

# Selecting Die Attach Technology for High-Power Applications

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Die attach is the process of making the electrical connection between the semiconductor device die and its package. Because it is the first packaging layer in contact with the die, its thermal characteristics are critical.

High-power semiconductor applications currently represent one of the highest growth sectors of any semiconductor technology, specifically because many of the key applications are driven by the creation or conservation of energy. These applications include motor control, HBLEDs, solar concentrator cells, and RF and microwave circuits used in radar and telecommunications equipment.

From a packaging perspective, there are a number of common requirements for all these high-power applications: they must handle high electrical currents, dissipate large amounts of heat, manage thermal expansion-induced stresses for high reliability, and this must all be accomplished at low cost. Cost, in this case, includes assembly as well as materials. ROHS regulations also add some new dimensions to these considerations.

## DIE ATTACH REQUIREMENTS

For most high-power semiconductor packaging geometries, the predominant heat dissipation path from the device is through the die attach material. Because the die attach layer is the first packaging layer in contact with the die, its thermal characteristics are the most critical. These characteristics include die attach layer thickness, thermal conductivity, and the thermal resistance at interfaces between the die attach, the device, and the package.

To provide a scale of the energy dissipation requirements, [Fig. 1](#) shows the energy dissipation in  $W/cm^2$  for some of the highest-power applications. This is the average power dissipation across the die, but local hot spots can have energy densities up to three times higher than the average.

Besides thermal dissipation, electrical conductivity is also a highly critical property for most high-power semiconductor applications. Electrical resistance between the die and the package results in joule heating, which is an energy-loss mechanism. Thus, the energy efficiency of the device is directly influenced by the electrical performance of the die attach layer, which is most critical for power semiconductors where the largest contribution to the critical  $R_{DS(ON)}$  parameter is typically the die attach layer. In this case, reducing the resistance of the die attach will reduce the magnitude of  $R_{DS(ON)}$  and improve the energy efficiency of the device.

For metals, both thermal energy and electrical current is carried by the same mechanism: electronic migration. Thus, the thermal and electrical conductivity of a metal-based die attach layer scales with each other (proportionately increase or decrease). Electrical resistance and thermal resistance will increase with rising temperature due to electron-phonon scattering.

The die attach layer is also the mechanical interface between the low thermal-expansion die (silicon 4.2 ppm/°C) and the packaging material. For die bonded to a copper paddle, for example, the copper temperature coefficient of expansion (TCE) is 17 ppm/°C. If TCE stress is large, portions of the die can go into tension and die cracking can result. To assess TCE stress, a number of key factors need to be taken into account:

- Die size
- Modulus of the die attach material
- Die attach temperature
- Curing temperature
- Package TCE
- Die attach pad-flatness specification
- Size of the die attach pad relative to die size and the shape of the die attach fillet
- Thickness of the die attach paddle (this determines how much bending of the paddle occurs during die attach)

[Fig. 2](#) shows a portion of a finite element model for a semiconductor die (blue) bonded to a high-expansion metal (yellow). The ends of the die are in tension (lighter tone color) and the rest of the device is in compression (darker tone color) due to TCE stress from the die attach process. Large tensile stresses in silicon cause die cracking, either after die attach or induced during post-assembly temperature cycling.

Another highly critical property for assessing die attach materials is the material and assembly cost. Material cost includes raw materials as well as die attach material fabrication. Assembly cost is very dependent on manufacturing throughput and yields. The sections that follow will illustrate that there is an extremely wide range in die attach material costs, ranging from more than \$15/g to less than \$0.10/g.

## DIE ATTACH MATERIALS

There are a wide range of die attach materials used in high-power applications, including materials on both sides of the performance spectrum: highly specialized materials for the highest-demand, niche applications, and very-high-volume materials typically used at the lower end of the performance scale. Gold-Silicon (AuSi) and Gold-Tin (AuSn) are both gold-rich eutectic compositions used in several distinct situations:

- To establish a solder hierarchy, both AuSi and AuSn have high melting temperatures (AuSi is processed at 420°C and AuSn at 350°C). [Fig. 3](#) shows the AuSi phase diagram. These

materials can be used for die attach in an assembly process where subsequent steps require additional high-temperature processing, such as a solder step at 260°C.

- Situations where flux use is not desirable. Both AuSn and AuSi can be used without flux in most circumstances (the exception is thick-film paste). Thus, for bonding die in a situation where tolerance for flux-associated contamination is very low, these materials are used.
- High thermal capability applications. AuSi in particular is a very high thermal-conductivity die attach layer (190 W/m-K).<sup>1</sup> AuSn has a thermal conductivity of 57 W/m-K, which is also higher than most other solder options. Both these materials also have correspondingly high electrical conductivity. AuSi is used for ultra-high thermal demand applications such as silicon LDMOS power amplifiers, where the local power dissipation can be as high as 3,000 W/m-K.

The major drawback for both of these materials is very high cost. Also, compared to other lower-temperature solders, AuSn and AuSi have low ductility, making TCE stress an issue, particularly when one considers the high die attach temperature. For example, Au<sub>80</sub>Sn<sub>20</sub> has a yield strength of 275 MPa (Mega Pascals).

From an assembly standpoint, AuSi cannot be deposited using plating and AuSn is difficult to plate. The most common deposition technology for these materials is pre-forms, thin-film deposition such as evaporation, jet vapor deposition<sup>2</sup>, or screen-printed thick-film pastes. AuSi can also be formed in situ by scrubbing the backside of a Si die with a thin Au metal layer onto a die attach pad that has been Au-plated. Since this reaction occurs above 400°C, the semiconductor device must be highly temperature resistant. AuSi is predominately used for high-power RF amplifiers which are bonded to expansion matched flanges.

Lead-tin (PbSn) remains one of the workhorse die attach materials for power semiconductors, particularly for large size die. In general, the high Pb formulations, such as Pb<sub>90</sub>Sn<sub>10</sub>, are widely used. The driving force of this material is a combination of high ductility and acceptable thermal conductivity for most applications. Pb<sub>90</sub>Sn<sub>10</sub> has a Young's modulus of 19 KN/mm<sup>2</sup>, elongation of 25% to 30%, and a thermal conductivity of 46 W/m-K.

Because of the highly ductile nature of Pb<sub>90</sub>Sn<sub>10</sub>, it minimizes the transfer of TCE stress between die and substrate during temperature excursions. This allows bonding of very large die without the risk of cracking. It also has 80% of the thermal conductivity of AuSn but costs 100 times less per weight. Pb<sub>90</sub>Sn<sub>10</sub> is also processed around 300°C, so it can also be used in a solder hierarchy with lower melting temperature solders for further assembly stages.

One significant issue of PbSn solder is its affect on health and the environmental. Currently there are no other alternative die attach materials that will work effectively for large, high-power die. Once these materials are developed, it is highly likely that PbSn will lose its current ROHS exception.

Another major drawback of PbSn is its slow throughput in automated die attach machines, due to the time required for the PbSn liquid to re-solidify after the die attach operation is completed. On the same die attach tool, PbSn throughput can be up to five times slower than epoxy-based die attach solutions.

Epoxy resin that has been highly loaded with silver metal flakes is another option for electrically conducting power-semiconductor die attach. Typically, silver-filled epoxy is used for smaller, lower-power die, but there are some exceptions to this trend. Most silver-epoxy die attach materials have a thermal conductivity between 2 and 12 W/m-K, but there are some much higher-performance materials.

There are two limiting factors for silver epoxy performance. One is the very high modulus of the material (for example, a dynamic tensile modulus of more than 3 gigapascals, GPa). This high modulus transfers large amounts of TCE stress from the substrate material to the die, and can result in die cracking. Thus, silver epoxy used for power applications is usually limited to smaller die to minimize this TCE stress effect. The largest die that can be used with a particular epoxy composition will also depend on the TCE of the substrate material that is utilized and the silver loading of the epoxy.

Another important issue with Ag-filled epoxy is the thermal resistance at the epoxy/die and epoxy/die attach pad interface. For solder material, this thermal resistance is very low as long as there is no voiding present. For Ag-filled epoxy, the bonding phase (epoxy) and the thermal conducting phase (Ag) are separate components of the die attach layer. Thus, any segregation of epoxy at the interface can result in a large interfacial thermal resistance, even for a highly thermally conductivity epoxy formulation.

The amount of segregation, and hence the interfacial thermal properties, are very dependent on the composition of the die attach material and the specific procedures used to apply the die attach layer. This sensitivity to processing becomes more of an issue as thermal conductivity of the Ag-filled epoxy increases. A thin thermally insulating layer is more of a performance issue for a 60-W/m-K material than it is for a 10-W/m-K material. The value of interfacial thermal resistance can be measured using a laser flash technique that will be discussed later.

[Fig. 4](#) is an SEM micrograph showing the metallization layer on a device and the underlying Ag-loaded epoxy. The dark areas in the picture denote the epoxy phase. The bright, flattened particles within the epoxy are the Ag flakes. At the top of the picture is the die metallization layer. It is clear from the picture that a portion of the interface between the die attach and the die metal is occupied by very low-thermal-conductivity epoxy. This epoxy layer influences both the thermal transfer and the  $R_{DS(ON)}$  value for power semiconductors.

## ORMET TLPS MATERIAL

Ormet transient liquid-phase sintered (TLPS) material<sup>[3]</sup> is a composite metal-based material that undergoes some dynamic structural changes during low-temperature heat treatment. It has been used for a number of years as a via-fill paste but is now being investigated as a die attach material. The die attach layer comprises three distinct metallic phases: pure copper, CuSn intermetallic compound phase, and Bi metal. There is also a small volume of an organic phase present, but at much lower levels than are seen in traditionally filled epoxy die attach. In [Fig. 5](#), the copper-colored phase is Cu, the dark grey is CuSn, and the light grey phase is the Bi. The dark isolated spots are the organic filler.

There are a number of key points which can be seen in the microstructure of [Fig. 5](#). First is the high volume of copper-containing phases. This is a key point because these phases carry both electrical current and heat conduction. A second key point is the clear metal-metal interfacial structure between the copper on either side of the die attach layer and the metal components (Cu, CuSn, and Bi phases) in the die attach layer. This metallic bonding between the die attach material and surrounding metal is the key distinguishing characteristic of the Ormet technology, and also results in low interfacial thermal resistance, as will be shown later.

The microstructure in [Fig. 5](#) is formed during a dynamic liquid-phase sintering process<sup>[4]</sup>. The as-deposited film contains an organic phase which acts as both a binder and a flux, a low-melting-temperature material such as SnBi and copper powder.

During processing, the low-melting SnBi alloy melts, enabling the Sn to create a fused inter-metallic network between the copper particles, the metallization on the back of the IC and the lead frame. The resulting continuous metal network is highly conductive and exhibits electrical and thermal stability above 265°C.

In the SnBi phase diagram in [Fig. 6](#), the 40/60 SnBi composition melts below 150°C, but once the Sn concentration is diminished, the Bi melting temperature is above 260°C. Thus, the TLPS material can be processed at a lower temperature but then forms a high-temperature composition that is consistent with Pb-free solder reflow.

Because of the presence of a continuous metallic phase, the thermal conductivity of the Ormet material ranges between 25 and 60 W/m-K<sup>[5]</sup>, very comparable to solder. From a mechanical standpoint, the material is less ductile than solder due to the presence of brittle CuSn inter-metallic compound (IMC) phases, but is more ductile than epoxy formulations.

The Ormet die attach material is only available as a thick-film paste that is screen-printed (dispensed) and dried, and then undergoes the sintering stage described above.

## WBC DIE ATTACH MATERIAL

Wafer backside-coated die attach material (WBC) is a new die attach film that has been developed at Henkel. One of the major distinguishing characteristics of WBC is that it is applied at the wafer level using screen printing, stencil printing, or spin coating. Coated wafers are shown in [Fig. 6](#).

Once applied, the die can be bonded using a standard die bonder in a process similar to traditional epoxy die attach, but without any dispense step. The advantage of this approach is lower manufacturing costs and very high manufacturing throughput. [Fig. 6](#) shows the WBC material coated on the backside of various wafers. Because the modulus of the WBC epoxy is similar to more standard epoxy, in general it is still not a reliable solution for large die where PbSn solder is typically utilized. The thermal conductivity is 11 W/m-K and the material is designed to bond to Ag, Cu, or Au metallization layers.

Another significant advantage of WBC is the highly uniform and thin die-attach-layer thickness, which can be achieved with wafer-level deposition. Bond line thicknesses of 20 μm can be achieved, ([Fig. 7](#)), which results in lower material usage compared to traditional Ag-filled epoxy, where a large fillet is formed. The smaller the die size, the more pronounced the material savings. Uniform die attach thickness also keeps the die very flat, which enhances upstream manufacturing processes such as wire-bonding.

## MATERIAL COMPARISONS

[Fig. 8](#) summarizes the thermal conductivity of the various power-semiconductor die attach materials. Besides thermal conductivity, another very critical thermal property is thermal interface resistance.

This is very low for solder materials (PbSn and AuSn) because a metallic bond is formed between the solder layer and the adjoining metallization. In some cases, however, the thermal resistance of silver-loaded epoxy can be high if there is an epoxy-rich region near the interface.

Thermal resistance of the Ormet material bonded to copper plates was measured using a laser-flash thermal conductivity measurement system. Using a one-dimensional heat-flow model and the

independently measured bulk thermal conductivity of the die attach material and adjoining layers (in this case Cu)  $\diamond$  the thermal contribution of the interfacial bonding regions can be determined<sup>[6]</sup>. The result of this measurement is shown in [Table 1](#).

The thermal conductivity shown in the second column of [Table 1](#) is the effective thermal conductivity of the Ormet die attach layer, including both the bulk thermal conductivity (60 W/m-K) and the interfacial thermal resistance. Stated a different way, the result of the interfacial thermal resistance is to lower the thermal conductivity of the entire layer (which includes both the bulk and interfacial regions) from 60 W/m-K to an effective thermal conductivity of about 35 W/m-K.

Clearly, for very high thermal applications, candidate die attach materials would be Ormet material, Pb90Sn10, and AuSn. [Table 2](#) compares these three materials using other important properties for high-power applications. The WBC and Ag-filled epoxy material are focused more on high volume, smaller die, and lower-cost applications for both discrete power semiconductors and power ICs. [Table 3](#) contrasts these two materials using important characteristics for high-volume assembly.

1. CMC measured the thermal conductivity of AuSi using laser flash.
2.  $\diamond$ Jet Vapor Deposition $\diamond$ , Peter Martin, *Vacuum Technology and Coating*, June 2009.

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5. Thermal conductivity measured at CMC using laser flash.
6. *Measurement of the Thermal Diffusivity of Translucent Aluminum Nitride*, R.C. Enck, R.D. Harris and R.A. Youngman,  $\diamond$ Advanced Characterization Techniques for Ceramics $\diamond$ , edited by W. Young Transactions, Vol. 5, American Ceramic Society, Westerville, OH, 1989, p. 214-222.

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